CLAIMS

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1. A network telephone comprising:

a microphone coupled to provide voice data to a network;

a speaker configured to facilitate listening to voice data from the network;

a dialing device coupled to facilitate routing of voice data upon the network;

a first port configured to facilitate communication with a first network device;

a second port configured to facilitate communication with a second network device; and

a prioritization circuit coupled to apply prioritization to voice data provided by the microphone.

2. The network telephone as recited in claim 1, wherein the first port is configured to facilitate communication of voice data packets with the first network device and the second port is configured to facilitate communication of voice data packets with the second network device.

3. The network telephone as recited in claim 1, wherein the microphone and the speaker at least partially define a handset.

4. The network telephone as recited in claim 1, wherein the dialing device comprises a keypad.

5. The network telephone as recited in claim 1, wherein the first port and the second port comprise Ethernet 10/100 ports.

6. The network telephone as recited in claim 1, wherein the prioritization circuit is defined by a network switch.

7. The network telephone as recited in claim 1, wherein the prioritization circuit is defined by an Ethernet switch.

8. The network telephone as recited in claim 1, wherein:

the prioritization circuit is defined by a network switch; and

further comprising a voice engine processor in communication with the network switch, the voice engine processor being configured to digitize and compress voice data from the microphone and to decompress and perform digital to analog conversion upon voice data provided to the speaker.

9. The network telephone as recited in claim 1, wherein:

the prioritization circuit is defined by a network switch; and

further comprising a voice engine processor in communication with the network switch, the voice engine processor being configured to digitize, compress and packetize voice data from the microphone and to depacketize, decompress and perform digital to analog conversion upon voice data provided to the speaker.

10. The network telephone as recited in claim 1, wherein the prioritization circuit is configured to tag voice data packets to facilitate prioritization thereof.

11. The network telephone as recited in claim 1, wherein the prioritization circuit is configured to tag voice data packets to facilitate prioritization thereof and is configured to read tags on data packets provided thereto by the network to facilitate prioritization thereof.

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12. A network telephone comprising:

a switch controller having at least one port for facilitating electrical communication with a network; and

a voice engine processor in electrical communication with the switch controller, the voice processor having a microphone port for facilitating electrical communication with a microphone and having a speaker port for facilitating electrical communication with a speaker.

13. The telephone as recited in claim 12, wherein the switch controller is configured to apply prioritization to voice packets.

14. The telephone as recited in claim 12, wherein the switch controller is configured to apply prioritization to voice data packets and to route voice data packets over a network.

15. The telephone as recited in claim 12, wherein the switch controller is configured to apply prioritization to voice data packets and to route voice data packets over an Ethernet.

16. The telephone as recited in claim 12, wherein the switch controller is configured to apply prioritization to voice data packets and to route voice data packets over the Internet.

17. The telephone as recited in claim 12, wherein the switch controller is configured to apply prioritization to voice data packets provided by the microphone and coupled to route the voice data packets over a network.

18. The network telephone as recited in claim 12, wherein the switch controller is configured to tag voice data packets to facilitate prioritization thereof.

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19. The network telephone as recited in claim 12, wherein the switch controller is configured to tag voice data packets to facilitate prioritization thereof and is configured to read tags on data packets provided thereto by the network to facilitate prioritization thereof.

20. The telephone as recited in claim 12, wherein the switch controller is configured to be compatible with Internet Protocol.

21. The telephone as recited in claim 12, wherein electrical communication between the switch controller and the voice engine processor is facilitated via a media independent interface and a microprocessor interface.

22. The telephone as recited in claim 12, wherein the switch controller comprises two ports for facilitating communication with the network.

23. The telephone as recited in claim 12, wherein the switch controller comprises two Ethernet ports for facilitating communication with the network.

24. The telephone as recited in claim 12, wherein the switch controller comprises two 10/100 megabit/sec Ethernet ports for facilitating communication with the network.

25. The telephone as recited in claim 12, wherein the voice engine processor further comprises a keypad port for facilitating communication with a keypad.

26. The telephone as recited in claim 12, wherein the voice engine processor further comprises a display port for facilitating communication with a display.

27. The telephone as recited in claim 12, wherein the switch controller is configure to be placed serially into a Ethernet transmission medium intermediate a network interface card and a switch.

28. The telephone as recited in claim 12, wherein the voice engine processor is configured to compress voice communications.

29. The telephone as recited in claim 12, wherein the voice engine processor is configured to compress voice communications using PCM compression.

30. The telephone as recited in claim 12, wherein the voice engine processor is configured to suppress silence.

31. The telephone as recited in claim 12, wherein the voice engine processor is configured to provide a desired level of quality of service.

32. The telephone as recited in claim 12, wherein the voice engine processor is configured to provide signaling for voice traffic.

33. The telephone as recited in claim 12, wherein the voice engine processor is configured to provide signaling for PBX voice traffic.

34. The telephone as recited in claim 12, wherein the voice engine processor is configured to provide echo control.

35. A network telephone comprising a prioritization circuit coupled to tag voice data packets with information representative of a priority thereof and coupled to read tags associated with packets.

36. A switch controller for controlling a network switch through which voice data is communicated, the switch controller comprising:

a packet buffer coupled to buffer voice data packets and non-voice data packets;

a switch engine queuing manager coupled to queue voice data packets and non-voice data packets in the packet buffer in a manner which enhances quality of service for the voice data packets;

at least one transceiver in communication with the packet buffer;

a network interface coupled facilitate communication between each transceiver and a network; and

a voice interface coupled to facilitate communication between a voice source and the packet buffer.

37. The switch controller as recited in claim 36, wherein the transceiver comprises a 10/100 transceiver.

38. The switch controller as recited in claim 36, further comprising a medium access control for each transceiver coupled to facilitate communication of voice packets and non-voice packets between the packet buffer and a network.

39. The switch controller as recited in claim 36, further comprising a 10/100 medium access control for each transceiver.

40. The switch controller as recited in claim 36, further comprising a medium access control coupled to facilitate communication of voice data packets between the voice source and the packet buffer via the voice interface.

41. The switch controller as recited in claim 36, further comprising a media dependent interface coupled to facilitate communication between each transceiver and the network.

42. The switch controller as recited in claim 36, further comprising a media independent interface coupled to facilitate communication between the packet buffer and the voice source.

43. The switch controller as recited in claim 36, further comprising a CPU interface coupled to facilitate communication between a CPU and the search engine queuing manager.

44. The switch controller as recited in claim 36, further comprising a CPU interface coupled to facilitate communication between a CPU and the search engine queuing manager, the CPU interface facilitating use of SNMP and BPDU frames.

45. The switch controller as recited in claim 36, further comprising a CPU interface coupled to facilitate communication between a CPU and the search engine queuing manager, the CPU interface having counters coupled to provide RMON support.

46. The switch controller as recited in claim 36, further comprising:

an address table; and

an address lookup engine couple to fetch addresses from the address table and to provide the addresses to the transceiver(s) to facilitate network routing.

47. The switch controller as recited in claim 36, further comprising:

a VLAN address table; and

an VLAN address lookup engine couple to fetch addresses from the address table and to provide the addresses to the transceiver(s) to facilitate network routing.

48. The switch controller as recited in claim 36, further comprising:

a display coupled to indicated a status of the switch controller; and

a display interface coupled to communicate status information to the display.

49. The switch controller as recited in claim 36, further comprising:

a plurality of LEDs coupled to indicated a status of the switch controller; and

an LED interface coupled to communicate status information to the LEDs.

50. The switch controller as recited in claim 36, wherein the switch engine queuing manager and the packet buffer are configured to cooperate so as to facilitate communication of network packets through the switch controller and to facilitate insertion of voice packets onto the network without blocking of the network packets.

51. The switch controller as recited in claim 36, further comprising an integrated address resolution unit coupled to provide medium access control addresses and VLAN tag resolution.

52. The switch controller as recited in claim 36, further comprising an integrated address resolution unit coupled to provide medium access control addresses and VLAN tag resolution at line rate.

53. The switch controller as recited in claim 36, further comprising an integrated address resolution unit configured to support ingress timestamp and egress delay flush.

54. The switch controller as recited in claim 36, further comprising an integrated address resolution unit configured to provide 256 medium access control addresses with a 16 bit tag.

55. A voice engine processor for use in network telephony, the voice engine processor comprising:

a CODEC;

a input port coupled to communicate an input audio signal from an input transducer to the CODEC;

an output port coupled to communicate an output audio signal from the CODEC to an output transducer;

a CPU; and

a DSP coprocessor coupled to the CPU so as to facilitate digital signal processing of voice data.

56. The voice engine as recited in claim 55, further comprising a microprocessor interface coupled to facilitate communication between the CPU and a switch controller.

57. The voice engine as recited in claim 55, wherein the CODEC comprises a 14 bit CODEC.

58. The voice engine as recited in claim 55, wherein the input port is configured to communicate a microphone output signal to the CODEC.

59. The voice engine as recited in claim 55, wherein the output port is configured to communicate an audio signal to a speaker.

60. The voice engine as recited in claim 55, further comprising:

a CPU;

memory in communication with the CPU;

a buffer; and

wherein the CPU is responsive to instructions stored in the memory so as to effect storage of information representative of at least one of the input audio signal and the output audio signal in the buffer.

61. The voice engine as recited in claim 55, further comprising:

a CPU;

memory in communication with the CPU;

a buffer in communication with the CPU; and

a digital signal coprocessor in communication with the CPU.

62. The voice engine as recited in claim 55, further comprising:

a serial port in communication with the CPU;

a general purpose input/output port in communication with the CPU;

a keyboard port in communication with the CPU; and

an LCD controller in communication with the CPU.

63. The voice engine as recited in claim 55, further comprising:

a serial port in communication with the CPU;

a general purpose input/output port in communication with the CPU;

a keyboard port in communication with the CPU;

an LCD controller in communication with the CPU;

a clock in communication with the CPU; and

an interrupt controller in communication with the CPU.

64. The voice engine as recited in claim 55, further comprising:

a peripheral bus in communication with the CPU via an IPB bridge;

a serial port in communication with the peripheral bus;

a general purpose input/output port in communication with the peripheral bus;

a keyboard port in communication with the peripheral bus;

an LCD controller in communication with the peripheral bus;

a clock in communication with the peripheral bus; and

an interrupt controller in communication with the peripheral bus.

65. The voice engine as recited in claim 55, further comprising:

a security module in communication with the CPU;

a DMA buffer in communication with the CPU;

a TDM interface in communication with the CPU; and

a MII interface in communication with the CPU.

66. The voice engine as recited in claim 55, further comprising:

a CPU bus in communication with the CPU;

a security module in communication with the CPU bus;

a DMA buffer in communication with the CPU bus;

a TDM interface in communication with the CPU bus; and

a MII interface in communication with the CPU bus.

67. The voice engine as recited in claim 55, further comprising:

a memory interface in communication with the CPU;

SDRAM in communication with the memory interface;

SSRAM in communication with the memory interface; and

flash ROM in communication with the memory interface.

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68. A network telephone system comprising:

a network; and

at least one network telephone, each network telephone comprising a network switch coupled to apply prioritization to voice packets and coupled to read prioritization of voice packets.

69. A method for communicating voice via a network, the method comprising:

facilitating routing of voice data upon the network via a dialing device;

providing voice data to a network via a microphone;

listening to voice data from the network via a speaker;

facilitating communication with a first network device via a first port;

facilitating communication with a second network device via a second port; and

prioritizing voice data provided by the microphone.

70. The method as recited in claim 69, wherein the first port is configured to facilitate communication of voice packets with the first network device and the second port is configured to facilitate communication of voice packets with the second network device.

71. The method as recited in claim 69, wherein the microphone and the speaker comprise a handset.

72. The method as recited in claim 69, wherein the dialing device comprises a keypad.

73. The method as recited in claim 69, wherein the first port and the second port comprise Ethernet 10/100 ports.

74. The method as recited in claim 69, wherein the prioritization circuit is defined by a network switch.

75. The method as recited in claim 69, wherein the prioritization circuit is defined by an Ethernet switch.

76. The method as recited in claim 69, wherein:

the prioritization circuit is defined by a network switch; and

further comprising a voice engine processor in communication with the network switch, the voice engine processor being configured to digitize and compress voice data from the microphone and to decompress and perform digital to analog conversion upon voice data provided to the speaker.

77. The method as recited in claim 69, wherein:

the prioritization circuit is defined by a network switch; and

further comprising a voice engine processor in communication with the network switch, the voice engine processor being configured to digitize, compress voice and packetize data from the microphone and to depacketize, decompress and perform digital to analog conversion upon voice data provided to the speaker.

78. The method as recited in claim 69, wherein the prioritization circuit is configured to tag voice packet to facilitate prioritization thereof.

79. The method as recited in claim 69, wherein the prioritization circuit is configured to tag voice packet to facilitate prioritization thereof and is configured to read tags on data packets provided thereto by the network to facilitate prioritization thereof.

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80. A method comprising:

using a switch controller having at least one port to facilitate electrical communication with a network; and

using a voice engine processor in electrical communication with the switch controller to process voice, the voice processor having a microphone port for facilitating electrical communication with a microphone and having a speaker port for facilitating electrical communication with a speaker.

81. The method as recited in claim 80, wherein the switch controller is configured to apply prioritization to voice packets.

82. The method as recited in claim 80, wherein the switch controller is configured to apply prioritization to voice packets and to route voice packets over a network.

83. The method as recited in claim 80, wherein the switch controller is configured to apply prioritization to voice packets and to route voice packets over an Ethernet.

84. The method as recited in claim 80, wherein the switch controller is configured to apply prioritization to voice packets and to route voice packets over the Internet.

85. The method as recited in claim 80, wherein the switch controller is configured to apply prioritization to voice packets provided by the microphone and coupled to route the vice packets over a network.

86. The method as recited in claim 80, wherein the switch controller is configured to tag voice packet to facilitate prioritization thereof.

87. The method as recited in claim 80, wherein the switch controller is configured to tag voice packet to facilitate prioritization thereof and is configured to read tags on data packets provided thereto by the network to facilitate prioritization thereof.

88. The method as recited in claim 80, wherein the switch controller is configured to be compatible with Internet Protocol.

89. The method as recited in claim 80, wherein electrical communication between the switch controller and the voice engine processor is facilitated via a media independent interface and a microprocessor interface.

90. The method as recited in claim 80, wherein the switch controller comprises two ports for facilitating communication with the network.

91. The method as recited in claim 80, wherein the switch controller comprises two Ethernet ports for facilitating communication with the network.

92. The method as recited in claim 80, wherein the switch controller comprises two 10/100 megabit/sec Ethernet ports for facilitating communication with the network.

93. The method as recited in claim 80, wherein the voice engine processor further comprises a keypad port for facilitating communication with a keypad.

94. The method as recited in claim 80, wherein the voice engine processor further comprises a display port for facilitating communication with a display.

95. The method as recited in claim 80, wherein the switch controller is configure to be place serially into a Ethernet transmission medium intermediate a network interface card and a switch.

96. The method as recited in claim 80, wherein the voice engine processor is configured to compress voice communications.

97. The method as recited in claim 80, wherein the voice engine processor is configured to compress voice communications using PCM compression.

98. The method as recited in claim 80, wherein the voice engine processor is configured to suppress silence.

99. The method as recited in claim 80, wherein the voice engine processor is configured to provide a desired level of quality of service.

100. The method as recited in claim 80, wherein the voice engine processor is configured to provide signaling for voice traffic.

101. The method as recited in claim 80, wherein the voice engine processor is configured to provide signaling for PBX voice traffic.

102. The method as recited in claim 80, wherein the voice engine processor is configured to provide echo control.

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103. A method for communicating voice via a network, the method comprising tagging voice packets with information representative of a priority thereof and reading tags associated with packets.

104. A method for controlling a network switch through which voice data is communicated, the method comprising:

buffering voice packets and non-voice packets;

queuing voice packets and non-voice packets in the packet buffer in a manner which enhances quality of service for the voice packets;

communicating voice packets from the packet buffer to at least one transceiver;

communicating voice packets between each transceiver and a network; and

communicating between a voice source and the packet buffer.

105. The method as recited in claim 104, wherein the transceiver comprises a 10/100 transceiver.

106. The method as recited in claim 104, further comprising a medium access control for each transceiver coupled to facilitate communication of voice packets and non-voice packets between the packet buffer and a network.

107. The method as recited in claim 104, further comprising a 10/100 medium access control for each transceiver.

108. The method as recited in claim 104, further comprising a medium access control coupled to facilitate communication of voice packets between the voice source and the packet buffer via the voice interface.

109. The method as recited in claim 104, further comprising a media dependent interface coupled to facilitate communication between each transceiver and the network.

110. The method as recited in claim 104, further comprising a media independent interface coupled to facilitate communication between the packet buffer and the voice source.

111. The method as recited in claim 104, further comprising a CPU interface coupled to facilitate communication between a CPU and the search engine queuing manager.

112. The method as recited in claim 104, further comprising a CPU interface coupled to facilitate communication between a CPU and the search engine queuing manager, the CPU interface facilitating use of SNMP and BPDU frames.

113. The method as recited in claim 104, further comprising a CPU interface coupled to facilitate communication between a CPU and the search engine queuing manager, the CPU interface having counters coupled to provide RMON support.

114. The method as recited in claim 104, further comprising:

an address table; and

an address lookup engine couple to fetch addresses from the address table and to provide the addresses to the transceiver(s) to facilitate network routing.

115. The method as recited in claim 104, further comprising:

a VLAN address table; and

an VLAN address lookup engine couple to fetch addresses from the address table and to provide the addresses to the transceiver(s) to facilitate network routing.

116. The method as recited in claim 104, further comprising:

a display coupled to indicated a status of the switch controller; and

a display interface coupled to facilitate communicate status information to the display.

117. The method as recited in claim 104, further comprising:

a plurality of LEDs coupled to indicated a status of the switch controller; and

an LED interface coupled to facilitate communicate status information to the LEDs.

118. The method as recited in claim 104, wherein the switch engine queuing manager and the packet buffer are configured to cooperate so as to facilitate communication of network packets through the switch controller and to facilitate insertion of voice packets onto the network without blocking of the network packets.

119. The method as recited in claim 104, further comprising an integrated address resolution unit coupled to provide medium access control addresses and VLAN tag resolution.

120. The method as recited in claim 104, further comprising an integrated address resolution unit coupled to provide medium access control addresses and VLAN tag resolution at line rate.

121. The method as recited in claim 104, further comprising an integrated address resolution unit configured to support ingress timestamp and egress delay flush.

122. The method as recited in claim 104, further comprising an integrated address resolution unit configured to provide 256 medium access control addresses with a 16 bit tag.

123. A method for processing voice for communication via a network, the method comprising:

communicating an analog input audio signal from an input transducer to an analog to digital converter to provide a digital input audio signal;

communicating a digital output audio signal to a digital to analog converter to provide an analog output audio signal to an output transducer; and

processing the digital input audio signal and the digital output audio signal with a DSP coprocessor coupled to the CPU.

124. The method as recited in claim 123, further comprising a microprocessor interface coupled to facilitate communication between the CPU and a switch controller.

125. The method as recited in claim 123, wherein the CODEC comprises a 14 bit CODEC.

126. The method as recited in claim 123, wherein the input port is configured to communicate a microphone output signal to the CODEC.

127. The method as recited in claim 123, wherein the output port is configured to communicate an audio signal to a speaker.

128. The method as recited in claim 123, further comprising:

a CPU;

memory in communication with the CPU;

a buffer; and

wherein the CPU is responsive to instructions stored in the memory so as to effect storage of information representative of at least one of the input audio signal and the output audio signal in the buffer.

129. The method as recited in claim 123, further comprising:

a CPU;

memory in communication with the CPU;

a buffer in communication with the CPU; and

a digital signal coprocessor in communication with the CPU.

130. The method as recited in claim 123, further comprising:

a serial port in communication with the CPU;

a general purpose input/output port in communication with the CPU;

a keyboard port in communication with the CPU; and
an LCD controller in communication with the CPU.

131. The method as recited in claim 123, further comprising:
a serial port in communication with the CPU;
a general purpose input/output port in communication with the CPU;
a keyboard port in communication with the CPU;
an LCD controller in communication with the CPU;
a clock in communication with the CPU; and
an interrupt controller in communication with the CPU.

132. The method as recited in claim 123, further comprising:
a peripheral bus in communication with the CPU via an IPB bridge:
a serial port in communication with the peripheral bus;
a general purpose input/output port in communication with the peripheral bus;
a keyboard port in communication with the peripheral bus;
an LCD controller in communication with the peripheral bus;
a clock in communication with the peripheral bus; and
an interrupt controller in communication with the peripheral bus.

133. The method as recited in claim 123, further comprising:
a security module in communication with the CPU;
a DMA buffer in communication with the CPU;
a TDM interface in communication with the CPU; and
a MII interface in communication with the CPU.

134. The method as recited in claim 123, further comprising:
a CPU bus in communication with the CPU;
a security module in communication with the CPU bus;

a DMA buffer in communication with the CPU bus;
a TDM interface in communication with the CPU bus; and
a MII interface in communication with the CPU bus.

135. The method as recited in claim 123, further comprising:
a memory interface in communication with the CPU;
SDRAM in communication with the memory interface;
SSRAM in communication with the memory interface; and
flash ROM in communication with the memory interface.

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136. A method for communicating voice comprising:
providing a network; and
applying prioritization to voice packets and reading prioritization of voice packets via at least one network telephone, each network telephone comprising a network switch.